

WHAT IS CLAIMED IS:

1. A data selection apparatus comprising:
search units each of which search units
- 5 includes table search circuits and a first circuit
which performs a first selection process in which a
table search circuit which outputs data is selected
from table search circuits each of which succeeds in
a search based on input data; and
- 10 a second circuit which performs a second
selection process in which a search unit which
outputs data is selected from search units each of
which includes a table search circuit which succeeds
in a search; wherein
- 15 when said first circuit receives a first
signal which indicates that there is a table search
circuit which succeeds in a search, said first
circuit sends a second signal to said second circuit
before performing said first selection process, said
20 second signal indicating that there is at least one
table search circuit which succeeds in a search;
said second circuit performs said second
selection process when said second circuit receives
said second signal; and
- 25 a search unit which is selected by said
second selection process outputs data.
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2. The data selection apparatus as claimed
in claim 1, wherein each of said search units has a
third circuit, outside of said first circuit, which
third circuit sends said first signal to said second
35 circuit; and
said first circuit performs said first
selection process at the same time as when said

third circuit sends said first signal to said second circuit.

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3. The data selection apparatus as claimed in claim 1, wherein each of said table search circuits is a CAM.

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4. The data selection apparatus as claimed in claim 1, wherein each of said table search circuits includes a RAM and an MPU.

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5. The data selection apparatus as claimed in claim 3, wherein said first circuit includes a CAM output control circuit including small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed; and said second circuit also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed.

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6. A data selection apparatus comprising:
search units each of which search units
comprises table search circuits and a data output
control circuit, said table search circuit selecting
data from a stored data table, which data includes

an entry matching a search key which is a bit sequence of a part of input data, said data output control circuit performing a first selection process in which the highest priority output data is

5 selected from outputs of said table search circuits; a unit output control device which performs a second selection process in which the highest priority output data is selected from outputs of said search units;

10 data search success signal output means which sends a data search success signal to said data output control circuit from a hit circuit which is a table search circuit which succeeds in a search; and

15 unit search success signal output means which sends a unit search success signal indicating that there is at least said hit circuit in said search unit to said unit output control device before said data output control device performs said

20 first selection process; wherein

25 said data output control device starts said first selection process upon receiving said data search success signal and said unit output control device starts said second selection process upon receiving said unit search success signal; and

a data output control circuit in a search unit which is selected by said unit output control device selects output data of a table search circuit.

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7. The data selection apparatus as claimed in claim 6, further comprising:

35 first stage search units each of which is said search unit;

nth ($n \geq 2$) stage search units each of

which nth stage search units includes (n-1)th stage search units and an (n-1)th stage unit output control device which selects the highest priority (n-1)th stage search unit from said (n-1)th stage

5 search units; and

an nth stage unit output control device which selects the highest priority nth stage search unit from said nth stage search units; wherein
said (n-1)th stage unit output control
10 devices send nth stage unit search success signals to said nth stage unit output control device before each of said (n-1)th stage unit output control device selects an (n-1)th stage search unit; and
an (n-1)th stage search unit output
15 selection process in said (n-1)th stage unit output control devices and an nth stage search unit output selection process in said nth stage unit output control device are performed in parallel so that output data of a table search circuit is selected.

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8. The data selection apparatus as claimed
25 in claim 7, wherein each of said first stage search units sends a unit search success signal to unit output control devices of second or later stages instead of (k-1)th ($2 \leq k \leq n$) stage unit output control devices sending said unit search success
30 signal to a kth stage unit output control device.

35 9. The data selection apparatus as claimed in claim 6, wherein said data output control circuit includes a CAM output control circuit including

small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed; and

5 said unit output control device also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed.

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10. The data selection apparatus as claimed in claim 7, wherein said data output control circuit includes a CAM output control circuit
15 including small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed; and

20 said unit output control device also includes small-scale logic circuits divided by flip-flops in which time series pipeline processing is performed

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11. The data selection apparatus as claimed in claim 6, wherein each of said table search circuits includes a RAM and an MPU.

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12. The data selection apparatus as claimed in claim 7, wherein each of said table
35 search circuits includes a RAM and an MPU.

13. A packet processing apparatus including a data selection apparatus, said data
5 selection apparatus comprising:

search units each of which search units includes table search circuits and a first circuit which performs a first selection process in which a table search circuit which outputs data is selected
10 from table search circuits each of which succeeds in a search based on an input packet; and

15 a second circuit which performs a second selection process in which a search unit which outputs data is selected from search units each of which includes a table search circuit which succeeds in a search; wherein

20 when said first circuit receives a first signal which indicates that there is a table search circuit which succeeds in a search, said first circuit sends a second signal to said second circuit before performing said first selection process, said second signal indicating that there is at least one table search circuit which succeeds in a search;

25 said second circuit performs said second selection process when said second circuit receives said second signal; and

30 a search unit which is selected by said second selection process outputs data, said data being used as a destination address to which said input packet is transferred.

35 14. The packet processing apparatus as claimed in claim 13, wherein each of said search units has a third circuit, outside of said first

circuit, which third circuit sends said first signal to said second circuit; and

 said first circuit performs said first selection process at the same time as when said

5 third circuit sends said first signal to said second circuit.

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 15. A packet processing apparatus including a data selection apparatus, said data selection apparatus comprising:

 search units each of which search units
15 comprises table search circuits and a data output control circuit, said table search circuit selecting data from a stored data table, which data includes an entry matching a search key which is a bit sequence of a part of an input packet, said data
20 output control circuit performing a first selection process in which the highest priority output data is selected from outputs of said table search circuits;

 a unit output control device which performs a second selection process in which the
25 highest priority output data is selected from outputs of said search units;

 data search success signal output means which sends a data search success signal to said data output control circuit from a hit circuit which
30 is a table search circuit which succeeds in a search; and

 unit search success signal output means which sends a unit search success signal indicating that there is at least said hit circuit in said
35 search unit to said unit output control device before said data output control device performs said first selection process; wherein

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5 said data output control device starts
said first selection process upon receiving said
data search success signal and said unit output
control device starts said second selection process
upon receiving said unit search success signal; and
a data output control circuit in a search
unit which is selected by said unit output control
device selects output data of a table search circuit,
said output data being used as a destination address
10 to which said input packet is transferred.

15 16. The packet processing apparatus as
claimed in claim 15, said data selection apparatus
further comprising:

20 first stage search units each of which is
said search unit;
nth ($n \geq 2$) stage search units each of
which nth stage search units includes ($n-1$)th stage
search units and an ($n-1$)th stage unit output
control device which selects the highest priority
($n-1$)th stage search unit from said ($n-1$)th stage
25 search units; and

an nth stage unit output control device
which selects the highest priority nth stage search
unit from said nth stage search units; wherein
said ($n-1$)th stage unit output control
30 devices send nth stage unit search success signals
to said nth stage unit output control device before
each of said ($n-1$)th stage unit output control
device selects an ($n-1$)th stage search unit; and
an ($n-1$)th stage search unit output
35 selection process in said ($n-1$)th stage unit output
control devices and an nth stage search unit output
selection process in said nth stage unit output

control device are performed in parallel so that output data of a table search circuit is selected.

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17. The packet processing apparatus as claimed in claim 16, wherein each of said first stage search units sends a unit search success
10 signal to unit output control devices of second or later stages instead of $(k-1)$ th ($2 \leq k \leq n$) stage unit output control devices sending said unit search success signal to a k th stage unit output control device.

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